CLAIMS

What is claimed is:

1. A multi-channel segmented resistor string digital to analog converter (DAC) comprising:

an A bit primary resistor string;

a plurality of buffer amplifiers, each buffering a respective node between resistors of the primary resistor string, outputs of the buffer amplifiers and ends of the primary resistor string defining $2^A + 1$ primary string nodes;

a plurality M of B bit secondary resistor strings, the nodes between resistors and ends of each secondary resistor string defining $2^B + 1$ secondary string nodes; and,

a plurality of primary string switches coupled to each primary string node, an output of each switch being coupled to an end of a respective secondary resistor string.

2. The DAC of claim 1 wherein the offset voltage of the buffer amplifiers is minimized by trimming.

3. The DAC of claim 1 further comprising M replica current sources, each coupled to a respective secondary resistor string, each replica current source providing a current through the respective secondary resistor string to cause a voltage across the respective secondary resistor

string equal to the voltage between adjacent primary string nodes.

4. The DAC of claim 1 wherein the number of primary string switches coupled to each primary string node is M, outputs of the switches being coupled together in groups to the ends of respective secondary resistor strings to controllably couple the ends of each secondary resistor string to any pair of adjacent primary resistor string nodes using leapfrogging.

5. The DAC of claim 4 further comprising M replica current sources, each coupleable to a respective secondary resistor string with either polarity, each replica current source providing a current through the respective secondary resistor string to cause a voltage across the respective secondary resistor string of a magnitude and a polarity equal to the voltage between primary string nodes to which the respective secondary resistor string may be coupled.

6. The DAC of claim 4 further comprised of:

M C bit tertiary resistor strings, nodes between resistors of each tertiary resistor string and ends of each tertiary resistor string defining $2^C + 1$ tertiary string nodes; and,

a plurality of secondary string switches, each coupled to a respective node of the secondary strings, each switch being coupled to an end of a respective tertiary resistor string.

7. The DAC of claim 6 wherein the resistance of each resistor in the tertiary string is greater than the resistance of each resistor in the secondary string.

8. The DAC of claim 6 further comprised of output select switches coupled to the nodes of each tertiary resistor string controllable to select the voltage on any one node of each tertiary resistor string node as a DAC output for a total of M DAC outputs.

9. The DAC of claim 6 wherein the number of secondary string switches coupled to each secondary string node is M, outputs of the secondary string switches being coupled together in groups to the ends of respective tertiary resistor strings to controllably couple the ends of each tertiary resistor string to any pair of adjacent secondary resistor string nodes using leapfrogging.

10. The DAC of claim 1 further comprised of:

M C bit tertiary resistors; and,

a plurality of secondary string switches associated with the nodes of the secondary strings, each switch being coupled to an end of a respective secondary resistor string.

11. The DAC of claim 10 wherein the number of secondary string switches coupled to each secondary string node is M, outputs of the secondary string switches being coupled together in groups to the ends of respective tertiary resistor strings to controllably couple the ends of each tertiary resistor string to any pair of adjacent secondary resistor string nodes using leapfrogging.

12. The DAC of claim 1 further comprising D bit resistor strings in parallel with the primary resistor string, where D is less than A, the D bit resistor strings being laser trimmed.

13. A multi-channel segmented resistor string digital to analog converter (DAC) comprising:

an A bit primary resistor string;

a plurality of buffer amplifiers, each buffering a respective node between resistors of the primary resistor string, outputs of the buffer amplifiers and ends of the primary resistor string defining $2^A + 1$ primary string nodes;

a plurality M of B bit secondary resistor strings, the nodes between resistors and ends of each secondary resistor string defining $2^B + 1$ secondary string nodes;

a plurality of primary string switches coupled to each primary string node, an output of each switch being coupled to an end of a respective secondary resistor string;

a plurality M of C bit tertiary resistor strings, nodes between resistors and ends of the tertiary resistor strings defining $2^C + 1$ tertiary string nodes for each tertiary resistor string;

a plurality of secondary string switches coupled to the nodes of the secondary strings, each switch being coupled to an end of a respective tertiary resistor string; and,

output select switches coupled to the nodes of each tertiary resistor string controllable to select the voltage on any one node of each tertiary resistor string node as a DAC output for a total of M DAC outputs.

14. The DAC of claim 13 wherein the offset voltage of the buffer amplifiers is minimized by trimming.

15. The DAC of claim 13 further comprising M replica current sources, each coupled to a respective secondary resistor string, each replica current source providing a current through the respective secondary resistor string to cause a voltage across the respective secondary resistor

string equal to the voltage between adjacent primary string nodes.

16. The DAC of claim 15 further comprising D bit resistor strings in parallel with the primary resistor string, where D is less than A, the D bit resistor strings being laser trimmed.

17. The DAC of claim 13 further comprising D bit resistor strings in parallel with the primary resistor string, where D is less than A, the D bit resistor strings being laser trimmed.

18. The DAC of claim 13 wherein the number of primary string switches coupled to each primary string node is M, outputs of the switches being coupled together in groups to the ends of respective secondary resistor strings to controllably couple the ends of each secondary resistor string to any pair of adjacent primary resistor string nodes using leapfrogging.

19. The DAC of claim 18 further comprising M replica current sources, each coupleable to a respective secondary resistor string with either polarity, each replica current source providing a current through the respective secondary resistor string to cause a voltage across the respective

secondary resistor string of a magnitude and a polarity equal to the voltage between primary string nodes to which the respective secondary resistor string may be coupled.

20. The DAC of claim 13 wherein the resistance of each resistor in the tertiary string is greater than the resistance of each resistor in the secondary string.

21. The DAC of claim 20 wherein the number of secondary string switches coupled to each secondary string node is M, outputs of the secondary string switches being coupled together in groups to the ends of respective tertiary resistor strings to controllably couple the ends of each tertiary resistor string to any pair of adjacent secondary resistor string nodes using leapfrogging.

22. The DAC of claim 21 wherein the number of secondary string switches coupled to each secondary string node is M, outputs of the secondary string switches being coupled together in groups to the ends of respective tertiary resistor strings to controllably couple the ends of each tertiary resistor string to any pair of adjacent secondary resistor string nodes using leapfrogging.

23. The DAC of claim 13 wherein the multi-channel segmented resistor string digital to analog converter is a single integrated circuit.

24. A method of multiple channel digital to analog conversion comprising:

providing an A bit primary resistor string;

providing M secondary resistor strings and M tertiary resistor strings;

selectively coupling adjacent pairs of nodes in the primary string to opposite ends of each secondary resistor string;

selectively coupling adjacent pairs of nodes in each secondary string to opposite ends of each tertiary resistor string; and,

selectively coupling one node in each tertiary resistor string, each as one output of the multiple channel digital to analog conversion.

25. The method of claim 24 further comprising coupling a D bit resistor string in parallel with the A bit resistor string, where D is less than A, and laser trimming the D bit resistor string.

26. The method of claim 25 further comprised of coupling a current source in series with each secondary resistor string, each current source providing a current through the respective secondary resistor string equal to the voltage difference between adjacent nodes in the first resistor string.

27. The method of claim 26 wherein selectively coupling adjacent pairs of nodes in the primary string to opposite ends of each secondary resistor string is done using leapfrogging, and wherein the polarity of the current sources is varied accordingly.

28. The method of claim 27 wherein the resistance of each resistor in the tertiary resistor string is selected to be greater than the resistance of each resistor in the secondary resistor string.

29. The method of claim 28 further comprised of buffering the nodes between resistors in the primary resistor string.

30. The method of claim 29 further comprised of minimizing the offset voltage of the buffer amplifiers by trimming.